

IMPLEMENTATION OF LOW POWER VLSI ARCHITECTURE FOR LOSSLESS COMPRESSOR AND DE-COMPRESSOR

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ABSTRACT

In this paper we present a compressor and de-compressor which is implemented for low power with GR algorithm using GSM technique. To implement the code compressor and de-compressor unit of the processor we have used the random signal and they are given to the ADC and to the lossless compressor and de-compressor block consists of GR unit. We were able to achieve the total power saving of 37.7% area increased for the compressor by 15.15%. Since the compressor is reducing the number of bits, while processing the area of the subsystems in the processor are reduced which in turn reduces the static power in processor. This compressor and decompressor unit is implemented using FPGA spartan3E and the same we implemented using cadence tool for ASIC flow with 180nm technology.

KEYWORDS: Compression Ratio, Data Compressor, Power